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REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 3 through 5, 7 through 15, and 17 through 21 are pending in this application. Claims 2, 6, 16, and 22 were previously cancelled. Claims 19 through 22 were previously added.

SECTION 103 ISSUES

In the Office Action, at paragraph 3, claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 stand rejected under 35 U.S.C. §103(a) as being anticipated by Huang, et al., U.S. patent number 6,131,134 (hereinafter *Huang*), in view of Rafferty et al., U.S. patent number 6,141,719 (hereinafter *Rafferty*) and Pollard, et al., U.S. patent number 5,754,870 (hereinafter *Pollard*). Applicant respectfully traverses.

Claim 1 now recites in pertinent part "controlling said switch with a detach control signal sent on a detach control signal wire separate from data transmission wires of said serial data bus *from a far end of* ***said*** *serial data bus* to cause an apparatus containing said first resistor and said switch to enter a logically detached state." (Applicant's emphasis added.) In the Office Action at paragraph 3, in reference to claim 1, it was admitted that "Huang does not teach said logically detaching control signal (e.g. switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus." The Office Action then states that "Rafferty discloses a USB selector switch, wherein a

logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13 - 29) is sent from a far end (i.e. from a corresponding peripheral module: See col. 3, lines 26 – 28) of a serial data bus (i.e. bus 14 of Fig. 3; See col. 2., lines 43 – 45)."

Rafferty Figure 4 is a detail of Figure 3, but Figure 4 has been confusingly presented geometrically reversed left-to-right. In order to more easily discuss the subject matter of *Rafferty*, applicant has prepared a sketch (attached) that combines Figures 3 and 4 with the details of Figure 4 shown in geometric order consistent with Figure 3.

The sketch shows a resistor Rpu and a pair of switches 24, 26 coupled to a near end of serial data bus (A), whose corresponding far side is in "downstream USB device 22". The switches have control signals "LS select" and "HS select". However, these control signals are *not* sent from the far side of serial data bus (A). *Rafferty* states at column 3, lines 24 to 28, that "the switches 24, 26 are controlled by data supplied from a corresponding peripheral module 12 based on the respective peripheral device 20 connected to the peripheral module 12 and by direction from the controller 18." *Rafferty* continues at column 3, lines 41 – 44, that "once the switch 10 is ready for operation, the switches 24, 26 are operated in accordance with the peripheral module 12, if any, that is communicating with the downstream module 16." Applicant has shown the controlling signal (data) from the peripheral module 12 to the switches 24, 26 as dashed lines E and F.

Applicant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16

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does *not* come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead *from the far end of a second data bus 14*. As the claim recites "said serial data bus", the controlling signal must come from the far end of the *same* serial data bus that is coupled to the resistor and switch. In the case of *Rafferty*, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a *different* data bus. Applicant therefore submits that the element of claim 1 under discussion is not taught by *Rafferty*.

Applicant therefore believes that independent claim 1 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 3 through 5, and 7, depend from independent claim 1, and because applicant believes that independent claim 1 is now allowable, applicant further believes that claims 3 through 5, and 7, are now allowable.

Claim 8 now recites in pertinent part "a detach control signal wire separate from data transmission wires of a serial data bus coupled to said switch at a near end of said serial data bus, to receive *a detach control signal sent from a far end of* ***said*** *serial data bus* to cause said apparatus to enter a logically detached state." (Applicant's emphasis added.) In the Office Action at paragraph 3, in reference to claim 8, it was admitted that "Huang does not teach said logically detaching control signal (e.g. switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus." The Office Action then states that "Rafferty discloses a USB selector switch, wherein a

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logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13 - 29) is sent from a far end (i.e. from a corresponding peripheral module: See col. 3, lines 26 – 28) of a serial data bus (i.e. bus 14 of Fig. 3; See col. 2., lines 43 – 45)."

The sketch attached to this response, as discussed previously, shows a resistor Rpu and a pair of switches 24, 26 coupled to a near end of serial data bus (A), whose corresponding far side is in "downstream USB device 22". The switches have control signals "LS select" and "HS select". However, these control signals are *not* sent from the far side of serial data bus (A). *Rafferty* states at column 3, lines 24 to 28, that "the switches 24, 26 are controlled by data supplied from a corresponding peripheral module 12 based on the respective peripheral device 20 connected to the peripheral module 12 and by direction from the controller 18." *Rafferty* continues at column 3, lines 41 – 44, that "once the switch 10 is ready for operation, the switches 24, 26 are operated in accordance with the peripheral module 12, if any, that is communicating with the downstream module 16." Applicant has shown the controlling signal (data) from the peripheral module 12 to the switches 24, 26 as dashed lines E and F.

Applicant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16 does *not* come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead *from the far end of a second data bus 14*. As the claim recites "*said* serial data bus", the controlling signal must come from the far end

of the *same* serial data bus that is coupled to the resistor and switch. In the case of *Rafferty*, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a *different* data bus. Applicant therefore submits that the element of claim 8 under discussion is not taught by *Rafferty*.

Applicant therefore believes that independent claim 8 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 9 through 15, and 17, depend from independent claim 8, and because applicant believes that independent claim 8 is now allowable, applicant further believes that claims 9 through 15, and 17, are now allowable.

Claim 15 now recites in pertinent part "means for controlling said switch with a detach control signal sent on a detach control signal wire separate from data transmission wires of said serial data bus *from a far end of said serial data bus* to cause said apparatus to enter a logically detached state." (Applicant's emphasis added.) In the Office Action at paragraph 3, in reference to claim 1, it was admitted that "Huang does not teach said logically detaching control signal (e.g. switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus." The Office Action then states that "Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13 - 29) is sent from a far end (i.e. from a corresponding peripheral module: See col. 3, lines 26 – 28) of a serial data bus (i.e. bus 14 of Fig. 3; See col. 2., lines 43 – 45)."

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The sketch attached to this response, as discussed previously, shows a resistor Rpu and a pair of switches 24, 26 coupled to a near end of serial data bus (A), whose corresponding far side is in "downstream USB device 22". The switches have control signals "LS select" and "HS select". However, these control signals are *not* sent from the far side of serial data bus (A). *Rafferty* states at column 3, lines 24 to 28, that "the switches 24, 26 are controlled by data supplied from a corresponding peripheral module 12 based on the respective peripheral device 20 connected to the peripheral module 12 and by direction from the controller 18." *Rafferty* continues at column 3, lines 41 – 44, that "once the switch 10 is ready for operation, the switches 24, 26 are operated in accordance with the peripheral module 12, if any, that is communicating with the downstream module 16." Applicant has shown the controlling signal (data) from the peripheral module 12 to the switches 24, 26 as dashed lines E and F.

Applicant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16 does *not* come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead *from the far end of a second data bus 14*. As the claim recites "said serial data bus", the controlling signal must come from the far end of the *same* serial data bus that is coupled to the resistor and switch. In the case of *Rafferty*, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a *different* data bus. Applicant therefore submits that the element of claim 15 under discussion is not taught by *Rafferty*.

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Applicant therefore believes that independent claim 15 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 16 through 21 depend from independent claim 15, and because applicant believes that independent claim 15 is now allowable, applicant further believes that claims 16 through 21 are now allowable.

Claim 19 now recites in pertinent part "a detach control signal wire separate from data transmission wires of said serial data bus coupled to said switch to receive a detach control signal sent from *said far end of said serial data bus* to said near end of said serial data bus." (Applicant's emphasis added.) In the Office Action at paragraph 3, in reference to claim 1, it was admitted that "Huang does not teach said logically detaching control signal (e.g. switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus." The Office Action then states that "Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13 - 29) is sent from a far end (i.e. from a corresponding peripheral module: See col. 3, lines 26 – 28) of a serial data bus (i.e. bus 14 of Fig. 3; See col. 2., lines 43 – 45)."

The sketch attached to this response, as discussed previously, shows a resistor Rpu and a pair of switches 24, 26 coupled to a near end of serial data bus (A), whose corresponding far side is in "downstream USB device 22". The switches have control signals "LS select" and "HS select". However, these control signals are *not* sent from the far side of

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serial data bus (A). *Rafferty* states at column 3, lines 24 to 28, that "the switches 24, 26 are controlled by data supplied from a corresponding peripheral module 12 based on the respective peripheral device 20 connected to the peripheral module 12 and by direction from the controller 18." *Rafferty* continues at column 3, lines 41 – 44, that "once the switch 10 is ready for operation, the switches 24, 26 are operated in accordance with the peripheral module 12, if any, that is communicating with the downstream module 16." Applicant has shown the controlling signal (data) from the peripheral module 12 to the switches 24, 26 as dashed lines E and F.

Applicant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16 does *not* come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead *from the far end of a second data bus 14.* As the claim recites "said serial data bus", the controlling signal must come from the far end of the *same* serial data bus that is coupled to the resistor and switch. In the case of *Rafferty*, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a *different* data bus. Applicant therefore submits that the element of claim 19 under discussion is not taught by *Rafferty.*

Applicant therefore believes that amended independent claim 19 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 20 and 21 depend from independent claim 19, and because applicant believes that independent claim 19 is now allowable, applicant further believes that claims 20 and 21 are now allowable.

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In the Office Action, at paragraph 7, it is stated that "it has been held that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference, nor is it that the claimed invention must be expressly suggested in any one or all of the references, but simply what the combination of references makes obvious to one of ordinary skill in the pertinent art. See *In re Bozek*, 163 USPQ 545 (CCPA 1969)". Applicant has not argued that *Pollard* may not be bodily incorporated into *Huang* and *Rafferty*. Applicant instead has argued that certain claim elements and limitations are not disclosed in any of *Huang*, *Rafferty*, and *Pollard*.

To establish a *prima facie* case of obviousness, case law requires three criteria.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicant submits that he has demonstrated that all the claim limitations are not disclosed in any of the combined references *Huang*, *Rafferty*, and *Pollard*.

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Moreover, the Federal Circuit has recently cautioned that the Patent Office must support its rejections for reasons that are stated on the record that establish why a particular combination would have been motivated by the prior art. It is inadequate to simply state in conclusory fashion that just because several elements existed in the prior art, that someone should have or would have been motivated to combine them. A specific teaching or a specific principle must be stated that makes the combination obvious.

> The need for specificity pervades this authority. See, e.g., In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references"). In re Sang Su Lee, 277 F.3d 1338, 61 USPQ 1430 (Fed. Cir. 2002).

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The Office Action, at paragraph 7, goes on to state that "in this present case, the Examiner has clearly pointed out rationale for appropriate combination of the references Huang, Rafferty, and Pollard." Applicant respectfully submits that there has been no rationale for combining the cited references. No "suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings" has been presented in the Office Action. Applicant submits that therefore a *prima facie* case of obviousness has not been made out in accordance with the *In re Vaeck* rule. There is no explanation of why someone of ordinary skill in the art would have selected and combined the cited references, as amplified above in the citation from *In re Sang Su Lee*. Applicant submits that the claimed invention of the present application is not made obvious by the mere existence and citation of the references *Huang*, *Rafferty*, and *Pollard*, even if they *had* in fact taught all the claim elements and limitations of the pending claims.

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SUMMARY

Applicant believes that all pending claims are allowable over the cited art of record. Applicant therefore respectfully requests that all pending claims 1, 3 through 5, 7 through 15, and 17 through 21 be allowed.

If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to contact applicant's representative, Dennis A. Nicholls, at (408) 765-5789.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

Date: March 30, 2004

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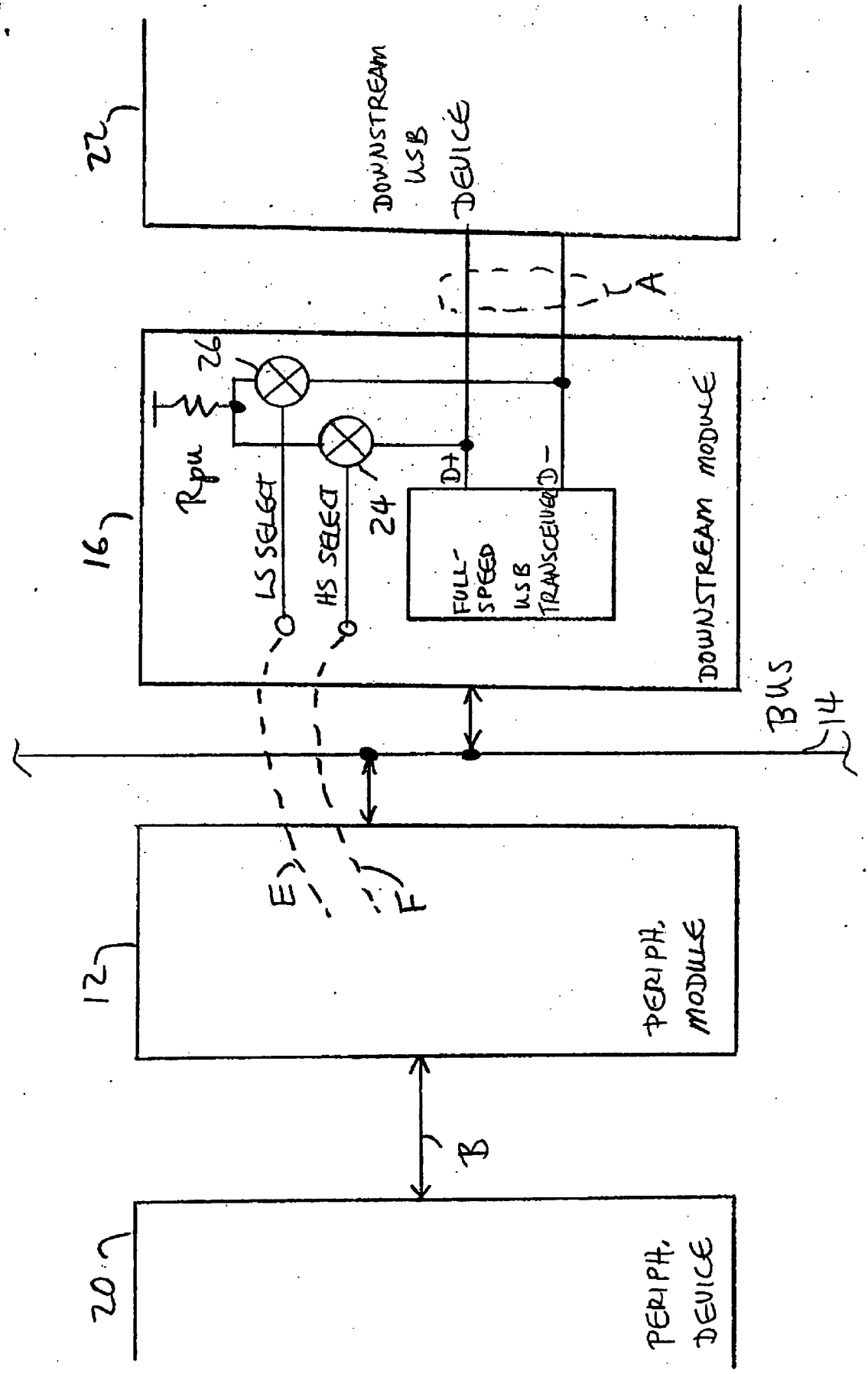

COMBINED FIGS. 3+4
US PAT # 6,141,719 "RAFFERTY"